(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 567 748 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 93104070.3

(51) Int. Cl.5: **G11B 5/64**, H01L 21/3205

(22) Date of filing: 12.03.93

(30) Priority: 10.04.92 US 866713

(43) Date of publication of application:
03.11.93 Bulletin 93/44

(84) Designated Contracting States:
DE FR GB

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(54) Fabrication and applications of rough silicon surfaces.

(57) The fabrication of rough Si surfaces with control of the roughness density, roughness length scale, and morphology on a nanometer scale is disclosed using 1) a low pressure chemical vapor deposition (CVD) process, typically in the 1 - 5 mTorr range, and 2) initial surface conditions and operating parameters such that initial growth is nucleation-controlled, e.g., using a thermal SiO_2 surface which is relatively unreactive to SiH_4 at an operating temperature below about 700 °C, and typically in the range of 500 - 600 °C. This broad temperature window enhances the feasibility of manufacturing rough silicon surfaces with broad applications. Further, various methods are presented for achieving surface pretreatment to control the size and density of the initial nuclei preparatory to the performance of the foregoing fabrication process. In addition, a method is disclosed for producing on a substrate surface, directly and in-situ, a pattern of submicrometer sized dots such that the dot center surface density and the total dot surface area coverage can be precisely controlled, using the features of the fabrication process with additional steps to achieve the desired dots.

Particular applications include fabricating rough Si surfaces as (1) electrodes for high capacitance density structures for high density DRAM and (2) as substrates for low-stiction magnetic disks.

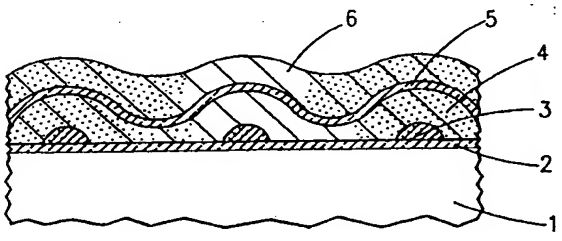

FIG.1D

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Field of the Invention

The present invention relates to the fabrication of semiconductor materials, and more particularly to a system and method for producing rough silicon surfaces with a precise level of control that renders them adaptable to wide application in computer-related devices, such as in VLSI chips and magnetic disks.

Prior Art

In semiconductor technology as the device dimensions are getting smaller it is becoming increasingly critical to be able to manipulate the surface topology of a substrate with control in the nanometer range Although this is possible in principle using state-of-the-art lithography techniques, these techniques are difficult to exploit in practice. In addition to the problems of photoresist handling, focus and depth-of-field, and proximity effects, nanolithography approaches suffer from low throughput, making them highly problematic for manufacturing applications.

A number of possible applications can be contemplated in which surface morphology may be tailored to advantage within the spatial regime of conventional and advanced lithography. In these cases, surface textures might be fabricated with some degree of randomness in their location. By exploiting such possibilities enhanced functionality for microelectronics applications can be gained. Three examples illustrate these possibilities.

A first example is the use of rough Si surface morphology, on the scale of ≤100nm feature sizes, to enhance capacitance density for capacitor applications like DRAM. The problem is that high levels of DRAM integration (e.g., 256 Mb or 1 Gb chips) necessitate smaller areas to hold each bit of information, but these smaller areas must provide higher capacitance per unit area. Recent publications, such as,
H. WATANABE, N. AOTO, S. ADACHI, T. ISHIJIMA, E. IKAWA, AND K. TERADA, "New stacked capacitor structure using hemispherical-grain polycrystalline-silicon electrodes", Appl. Phys. Lett. 58 (3), 251 (1991). (NEC Corp), M. SAKAO, N. KASAI, T. ISHIJIMA, E. IKAWA, H. WATANABE, K. TERADA, AND T. KIKKAWA, "A capacitor-over-bit-line (COB) cell with a hemispherical-grain storage node for 64Mb DRAMs", IEDM 90-655, 27.3.1 (1990). (NEC Corp), and M. YOSHIMARU, J. MIYANO, N. INOUE, A. SAKAMOTO, S. YOU, H. TAMURA, AND M. INO, "Rugged surface poly-Si electrode and low temperature deposited &Si3N4. for 64 Mbit and beyond STC DRAM cell", IEDM 90-659, 27.4.1 (1990). (OKI Corp), disclose results on the growth of rough polySi surfaces that show effective area enhancement (~2.5X) for given capacitor area, since within a given macroscopic area the rough surface texture provides more actual surface area. Rough surface texture is attractive when compared to its alternatives, namely (i) thinner insulator layers (which suffer from tunneling currents as well as much more difficult defect density considerations) and (ii) insulators of higher dielectric constant (which require fundamentally new materials and processes). On the other hand, a major concern is that the temperature window for growth of polySi with rough surface morphology has in prior art been very limited, extending only over ~10°C. Such tight temperature control is a problematical constraint on manufacturability. The explanation for the cause of rough surface morphology has been the occurrence of growth temperatures at the boundary between the amorphous and polySi microstructures. If this explanation is correct, a broader temperature process window using this mechanism would be unlikely. However, manufacturability concerns make it essential to develop processes with considerably broader temperature windows.

A second example, in a comparatively remote application, is the use of rough Si surfaces for the fabrication of low-stiction magnetic disk surfaces for storage applications. In order to minimize mechanical friction - especially at starting - disk surfaces are normally roughened before deposition of the magnetically active thin film, but the physical techniques presently used involve metallic substrates, which suffer from problems of topographic control as well as gouging and corrosion. New approaches which provided better control over morphology and its reproducibility, especially on a nanometer scale, would be of real benefit.

A third example is the exploitation of quantum effects in nanometer Si wires or dots which then permit significant light emission to occur in Si structures. See, for example, L.T. CANHAM, "Silicon quantum wire array fabrication by electrochemical and chemical dissolution of wafers", Appl. Phys. Lett. 57 (10), 1047 (1990).

The common theme in these three somewhat disparate examples is the desirability of a method for fabricating Si surfaces of controlled, predictable morphology with roughness length scales in the nanometer regime. Such rough Si surfaces would in all three cases be of real benefit when incorporated into larger, lithographically-defined microelectronic structures. Since the benefits of these rough Si applications do not require precise control of where the features (e.g., peaks or valleys in the topography) are found within lithographic dimensions, significant elements of statistical randomness can be accommodated. This factor opens

the door to a new range of chemical and physical processes and structures. The manufacturability of such structures would require not only high reproducibility but also good control over the density and shape of rough nanoscale features, irrespective of actually where they appeared on the surface. It should be clear that conventional lithography (e.g., electron beam) would require impossibly long exposure time to write similar features.

Plasma processes are capable of forming particles in the gas phase, and this has been suggested - together with directional etching for pattern transfer - as a means to generate random nanostructures on a surface. For instance, see G. S. SELWYN, G. S. OEHRLEIN, AND Z. A. WEINBERG, "Controlled surface texturing of materials", IBM TDB Vol.34, No.5, pps. 381-2, October, 1991. However, this approach yields a particle size distribution which is fairly broad, leading to a similar distribution of nanostructure sizes on the surface.

It is therefore the object of the present invention and highly desirable to provide an alternate, non-lithographic approach using a deposition or etching system to fabricate surface textures with random, nanometer-scale roughness. While the location of individual features (e.g., peaks) can be random, it is also highly desirable to control such parameters of these features as their density, their local shape, and their average size.

These objects are basically solved in advantageous manner by applying the features as laid down in the independent claims. Further advantageous developments are contained in the related subclaims.

The present invention involves the fabrication of Si surfaces with rough morphology on a nanometer scale using deposition (and in some cases etch) processes which control the roughness density, roughness length scale, and morphology. Further, the existence of the rough morphology does not depend critically on the process temperature, thereby offering a process which is much more readily utilizable in manufacturing than prior art processes for this purpose.

In accordance with the invention, a system and method are provided for fabricating a rough Si surface texture by using 1) a low pressure chemical vapor deposition (CVD) process, i.e., typically at a pressure in the 1 to 5 mTorr range, and broadly in the range from about 0.1 to 100 mTorr, and/or 2) initial surface conditions such that initial growth is nucleation-controlled, e.g., using a thermal SiO_2 surface which is relatively unreactive to SiH_4 at an operating temperature below about 700 °C permitting operating temperatures in an expanded range of ≥100 °C. The low pressure is believed to prevent excessive deposition of small gas-phase-nucleated particles, which would cause a smooth surface rather than the roughness desired. The broad temperature window obtained contrasts with the narrow, less than 10 ° window permitted by prior art processes.

Further, the invention involves various methods for achieving surface pretreatment to control the size and density of the initial nuclei preparatory to the performance of the foregoing fabrication process.

In addition, the invention includes a method to produce on a substrate surface, directly and in-situ, a pattern of submicrometer sized dots such that the dot center surface density and the total dot surface area coverage can be precisely controlled, using the features of the above-described process with additional steps to achieve the desired dots.

Finally, particular applications of the system and method as suggested above include fabricating rough Si surfaces as (1) electrodes for high capacitance density structures for high density DRAM and (2) as substrates for low-stiction magnetic disks. In both cases, the rough Si surfaces are prepared by (a) choosing or fabricating a surface which is chemically inert with respect to silane exposure at operating temperatures broadly in the range from about 450 °C to about 700 °C, and typically in the range of 500 - 600 °C, so that growth will be dominated by nucleation at specific defect sites, and (b) selectively growing Si on the distinct nucleation sites so as to enhance and transfer the morphology pattern of the nucleation sites into a thicker, rough Si film. Appropriate selection of deposition parameters, e.g., growth temperature, pressure, and initial surface condition, and of reactant species, SiO_2 and silane, provide preferred embodiments of the inert initial surface and reactant, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) through 1(d) are sectional views of a substrate surface illustrating a process sequence for the formation of a planar capacitor structure with high capacitance density fabricated in accordance with the present invention.

Figure 2 is a sectional view of a low-stiction surface on a magnetic disk having a rough silicon layer produced in accordance with the present invention disposed between the substrate and the magnetic surface layer with the rough silicon in the form of a series of random Si islands.

Figure 3 is a sectional view of a low-stiction surface on a magnetic disk having a rough silicon layer produced in accordance with the present invention wherein the rough silicon layer completely covers the substrate surface.

Figure 4 is a plot illustrating the growth in time of Si nuclei, produced in accordance with the

present invention, as a function of temperature at a pressure of 1.6 mTorr, and showing clearly that the surface area coverage by Si dots can be controlled by these parameters.

Figures 5(a) through 5(d) are sectional views of a substrate surface illustrating a process sequence for the formation of Si quantum dots for light emitting structures in accordance with the invention.

Figure 6 is a plot of surface area coverage by grown nuclei in accordance with the invention as a function of deposition time at a temperature of 550 °C for deposition pressures of 1.6 and 3.2 mTorr.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The present invention involves systems and methods by which the temperature process window for the growth of rough Si surface textures is expanded to ≥100 °C, as compared to prior processes wherein the process window was limited to less than 10 °C. The key factors in achieving a significantly broader process window are: (1) the use of very low pressure CVD conditions in the regime of about 0.1 to 100 mTorr, as contrasted with conventional LPCVD at ≥200 mTorr; and/or (2) initial surface conditions which favor nucleation-controlled growth. The ability to achieve this much larger process window greatly enhances the feasibility of manufacturing rough silicon surfaces with broad applications.

More particularly, previous work to grow rough polySi films was carried out under fairly standard LPCVD SiH_4 growth conditions, i.e. ≥200 mTorr, in a standard hot-wall LPCVD reactor. The present invention achieves a substantially broader temperature window (≥100 °C) for rough Si growth by employing a very different approach. First, very low pressure conditions are used, e.g., ~1 mTorr undiluted SiH_4. Such a pressure regime is inaccessible with conventional LPCVD tools and processes and thus normally would not be contemplated by those skilled in the art of polysilicon deposition using standard LPCVD conditions. The low pressure is believed to be important in order to minimize gas phase reaction, which could lead to deposition of very small particles and hence smoothing rather than roughening of the growth surface. Second, additionally or alternatively, the initial surface condition is chosen so that initial growth is nucleation-controlled, e.g., using a thermal SiO_2 surface which is relatively unreactive to SiH_4 in this temperature regime. Heretofore, initial nucleation has not been identified as an important factor in the growth of rough Si surfaces. Nucleation at the initial stages of growth is important in that it ultimately determines the topography of the rough Si films.

The two factors noted suggest that the growth of rough Si surfaces should involve basically two stages:

- *Generation of initial nuclei.*
  Initial nuclei growth should be low density. By using surface conditions which cause nucleation-controlled initial growth, a low density (~10^{10}/cm^2) of Si nuclei can be formed on the surface. This is, for example, the case for the SiH_4 reaction on thermal SiO_2 in the temperature range ~500-600 °C. The use of very low pressures, in the range ~1 mTorr, prevents gas phase reaction and particle formation, so that higher densities of Si nuclei are not deposited on the surface.
  It is believed that the use of very low pressures is important in preventing excessive deposition of gas-phase-nucleated particles on the surface, since large numbers of microparticles would form a fairly smooth surface as commonly obtained in conventional LPCVD polySi (except for very special, narrow temperature regimes). Here, a relatively low density of nuclei is established (~10^{10}/cm^2) to form a roughness template; and, once the surface is sufficiently covered, the growth is dominated by size increase in the Si nuclei, which largely replicates the roughness of the inital template.
  Because nucleation and subsequent very low pressure growth can both occur and be controlled over a broad temperature range, it is possible to obtain a substantial (~100 °C) temperature process window for rough Si growth. In contrast, previous work has involved the production of rough Si only over a much narrower temperature window corresponding to the amorphous/polycrystalline transition temperature - a very different growth mechanism.
  As described below, reasonable initial nuclei densities (~10^{10}/cm^2) are obtained using thermal SiO_2 surfaces, and a number of other approaches to establishing useful initial nuclei densities can be envisioned, such as a more highly defective oxide layer like native oxide, or impurity dosing (oxygen, carbon, etc.). Furthermore, it has been found that the roughness length scale (or initial nuclei density) can be varied significantly by variations in temperature and in pressure or residence time of reactant species in the reactor. This leads to tradeoffs which optimize microstructure/topography against growth rate, etc.
- *Growth of rough Si film from initial nuclei.*
  Once Si nuclei are present on the surface, the selectivity of SiH_4 growth plays a key

role. The SiH_4 reaction on Si is much faster than on SiO_2, so that once sufficient Si surface area has been established by the deposited nuclei, most subsequent Si deposition will take place on the nuclei and cause the surface morphology of the film to replicate the pattern of initial nuclei. Because very low pressures are used, gas phase nucleation and particle generation do not contribute significantly to film growth and morphology. In effect, then, the growth of Si from the original nuclei established represents a pattern transfer from a two-dimensional array of nuclei to a rough topography of the final Si film.

While adequate results for some purposes may be obtained using either of the two noted factors alone, experimental results and observations do suggest that rough Si surfaces could not be obtained over a broad growth temperature regime if higher pressures are used. At higher pressures, gas phase nucleation produces large densities of Si nuclei (microparticles) on the surface, leading to smoother morphology (much smaller grains at much higher density). Consequently, it is important to assure a low initial nuclei density and its morphological replication in the grown film.

Although Si surface mobility above the amorphous/crystalline transition temperature will change surface morphology somewhat (e.g., lead to faceting), the strong difference in reaction probability for SiH_4 on Si vs. SiO_2 assures that rough Si surfaces result over a broad growth temperature range.

In any event, it is highly desirable to attain independent control of the initial nuclei density irrespective of the growth conditions used to determine final nuclei sizes. To this end, improved control of the nuclei sites and density in the first step of surface fabrication may be achieved as follows.

Surface fabrication

In a first embodiment, surface treatments may be used to determine the density of sites for nucleation. Such treatments may be effective in enhancing nucleation from the very low pressure growth process at those sites, by:

(i) deposition of impurities (carbon, metal, oxygen, etc.) from gas phase exposure (e.g., acetylene for carbon deposition), liquid exposure (dips), or physical vapor deposition (e.g., evaporation or sputtering);

(ii) creation of defects by ion implantation, x-ray radiation, ion etching/bombardment, UV light to break surface bonds, etc.;

(iii) chemical modification of the surface, e.g., by growth of incomplete or defective layers like oxide, use of different growth techniques for these layers, etc.; and

(iv) growth of a full surface layer, such as native oxide, thermal oxide, CVD nitride, plasma-enhanced CVD (PECVD) dielectric, etc.

All such treatments will offer different site densities for nucleation.

In an alternate embodiment, actual nuclei may be deposited on the surface rather than altering the surface to form favorable sites for nucleation. For instance, elevating the pressure and/or temperature for a brief time (cf., the steady-state nuclei growth condition) may be used to form microparticles or higher precursor species in the gas phase, which then deposit onto the surface as real nuclei. Following this "seeding" of the surface, these initial nuclei at controlled densities may be subjected to further growth by very low presssure CVD.

In view of the foregoing control of the formation of initial nuclei density, growth may be limited to specific regions of the surface (e.g., ion implantation with a mask present) at least in some cases, leading to the possibility of patterning the resulting rough Si topographic regions.

In an actual implementation rough Si surfaces were produced by the SiH_4 CVD growth of Si films ~100nm thick in an ultraclean (UHV base pressure), cold-wall, rapid thermal CVD (RTCVD) reactor at pressures in the range ~1 mTorr, where gas phase nucleation should be small (see B.MEYERSON, J.JASINSKI, J. Appl. Phys. vol.61, p.785 (1987)). Deposition was initiated on thermal SiO_2 films ~20nm thick, leading to small densities of nucleation centers (~10^1 */cm^2). More details are described below in the section entitled *Nanometer–size Si dots*.

Scanning electron microscope (SEM) micrographs of the resulting surfaces were made and showed profound roughness for growth temperatures ranging from 510 to 570 °C. This temperature range is ≥6X broader than that previously achieved for growth of rough polySi at the boundary between amorphous and polycrystalline Si growth. With higher growth temperature, there is increasing evidence of facets on the polySi "bumps" demonstrating that roughness has been produced rather independently of surface diffusion associated with Si grain growth. This is a clear indication that the roughness mechanism employed here is not the amorphous-crystalline transition discussed in the prior art.

Preliminary observations have also been made at other temperatures, e.g., ~480 °C and ~600 °C, and have found quite similar rough morphology of the Si film, suggesting that the temperature window for rough Si growth is ≥100 °C, typically from about 500 to 600 °C, and anywhere in the range from about 450 to 700 °C.

Cross-sectional SEM micrographs suggest strongly that the rough surface morphology in the present invention results from additive pattern transfer due to growth at initial nucleation sites on the SiO_2 substrate surface.

Examples of applications in which specific embodiments of the invention may be used to advantage will now be described.

High-capacitance density DRAM structures

By growing a rough Si thin film as described above, a controlled increase in effective available surface area may be achieved. Use of this surface as the bottom electrode in a capacitor structure, will increase the capacitance for given macroscopic capacitor area. The invention may thus be applied in chip manufacturing in the DRAM and/or optoelectronics areas. Alternative solutions, such as plasma particulate generation for micromasking, offer less flexibility because dot density and size are linked by a single process (e.g., gas phase particle formation).

When applied in environments where DRAM or related device structures are required, the approach is particularly valuable to achieve manufacturability at very high integration levels (e.g., 256 Mb or 1 Gb) due to the process control and latitude available. For example, the above-mentioned ability to control nuclei density and to tailor the shape of nuclei (e.g., faceting) offers the potential to realize high capacitance enhancement with small nuclei of high density (very fine grain roughness) and aspect ratio. With a large number of nuclei in each capacitance cell, the distribution of capacitance values will be narrower, permitting higher yield at high integration levels.

It is important to note that current DRAM designs employ either stacked or trench capacitor configurations, in which much of the capacitor surface is in fact vertical. Since the oxidation and rough Si CVD deposition processes are conformal, i.e., involve reaction at sidewalls as well as on horizontal surfaces, fabrication of rough Si surfaces can be readily accomplished in the relevant geometries for advanced DRAM capacitor structures.

Accordingly, trench, stacked, or planar capacitor structures with high capacitance density may be fabricated by, referring to Figure 1(a), firstly treating the surface 2 of a substrate structure 1 so as to render it relatively inert with respect to reaction with Si-containing species, e.g., using a thermal SiO_2 layer thereon. Next, as shown in Figure 1(b), a Si-depositing-gas is used for depositing Si nuclei 3 on the surface 2. The density of the Si nuclei 3 formed on the substrate surface 2 is controlled by regulating the temperature and pressure conditions during deposition. It has been found that operating pressures can be below 200 mTorr and may range broadly from about 0.1 mTorr to 100 mTorr, with the preferred range being about 1 to 5 mTorr. The operating temperature can be below about 700 °C, and typically in the range of 500 - 600 °C and as low as about 450 °C.

As seen in Figure 1(c) further Si is then grown on the deposited nuclei 3 in order to produce a nearly continuous film 4 of Si with rough surface texture on the substrate structure. A thin conformal dielectric 5 is then formed over the rough Si surface of film 4, and finally, a Si top electrode 6 is deposited over the dielectric 5 to complete the capacitor structure as illustrated in Figure 1(d).

Hence, the invention is clearly applicable to DRAM technology and manufacturing, where enhanced capacitance density is a key driver. Other applications in high capacitance structures may include decoupling capacitors in high performance bipolar technology, or storage capacitors for thin film transistor liquid crystal display technology.

Low-stiction magnetic disks

A particularly valuable application of the present invention is in connection with magnetic disk manufacturing. The disclosed techniques are suitable for use in fabricating a passive topographic surface of controlled roughness on a 100 nm length scale as a substrate for low-stiction thin magnetic disk surfaces.

The reliability of thin film magnetic disk technology is limited by stiction between head and disk at start-up. To reduce stiction, disk surfaces are normally roughened prior to the deposition of a magnetically active thin film. Known technologies for producing low-stiction surfaces suffer from at least two shortcomings. First, the roughness characteristics are difficult to control on a nanometer scale; and, second, roughness is currently generated by physical means (e.g., operating tape, similar to sandpaper), which are limited in application to metallic substrates. In such case, defect densities are high due to (i) the generation of excessively large asperities associated with gouging of ductile metals and (ii) corrosion associated with galvanic action. Advancement in low-stiction technology requires better control of the roughness characteristics and statistics as well as applicability to insulating, passive substrates (e.g., glass) where advantages of lower cost and higher reliability are expected.

In accordance with the present invention, the formation of controlled roughness is based on the nucleation and early growth of Si islands by chemical vapor deposition. As desired, the surface of the substrate may be completely or incompletely covered by the depositied silicon. Two such configura-

tions are illustrated schematically in Figures 1 and 2; the former showing incomplete coverage, and the latter showing complete coverage of the substrate surface. As seen in the Figures, a suitable disk substrate 10 is provided to receive the rough silicon to be deposited. The deposition may be controlled as described herein to produce a series of random Si islands 12 as in Figure 2 or a rough continuous surface 14 as in Figure 3. After the processes described herein to form such a rough Si surface are completed a conformal magnetically active layer 16 can be deposited to achieve the low-stiction disk surface desired. Si deposited on thermal SiO_2 at a temperature of ~550°C at ~2 mTorr SiH_4 pressure displays morphology which can serve as a suitably roughened substrate for the conformal thin film magnetic layer of a disk. It should be noted that the roughness length scale in these cases is ~100 nm, with aspect ratio ~1, as presently required for low-stiction disk technology.

Nanometer–size Si dots

It will be seen from the foregoing descriptions that nanometer-size Si dots may be formed from very low pressure Si CVD, e.g., ~0.1 to 100 mTorr, by a two-step sequence:

(1) generation of nuclei at desired density; and

(2) controlled growth to desired coverage (average dot size or diameter).

The pattern of dots can then be transferred into the substrate, e.g., by etching, for a variety of applications where nanometer-scale features are required.

It is a further feature of the present invention to separate the processes for defining dot density and dot size (or area coverage) and control each independently. The preferred embodiment in this regard employs very low pressure SiH_4 CVD for both steps in sequence within the same reactor. First, a desired density of nuclei is produced on the surface. Second, very low pressure CVD is used to enlarge these small nuclei to the desired size.

In the preferred embodiment, this sequence encompasses the following procedures:

- Beginning with a well-defined substrate surface (e.g., thermal SiO_2) and low defect density (few nucleation sites), a large density of nuclei is then generated on the surface. One way to achieve this is to generate very small particles (or precursor molecules like disilane) during silane CVD at elevated pressure, which then deposit as seed nuclei on the surface. A second approach would be to form nuclei on the surface by heterogeneous reaction and to control their size and density distribution through the deposition parameters (temperature, pressure). Within the second approach, other surface pretreatments (e.g., native oxide, ion bombardment, etc.) could be employed to vary the nucleation site density in a controlled way.
- Once the desired density of nuclei has been established on the surface, Si deposition from SiH_4 (or other reactants) is carried out (e.g., at very low pressure) to cause 3-dimensional growth of Si nanostructural features at the nucleation sites. If very low pressures are employed, generation of new nucleation sites will be negligible. Furthermore, if the initial nuclei are very small, the size distribution of grown Si dots will be sharp, and average dot size will be closely controlled by growth conditions (temperature, time, actual pressure, etc.).

After the desired Si dot density and area coverage have been obtained, directional plasma-based etching may be used to transfer the pattern into the surface, as described in the previously-cited IBM TDB of G. S. SELWYN ET AL, and below. It should be noted that the fabrication of these nanostructural features is accomplished in-situ, including definition and fabrication of features without resist processing.

More specifically, the above SiH_4-based CVD embodiment has been used to grow a well-defined density of Si nuclei on a 20nm thermal SiO_2 layer using ultrahigh-vacuum-based rapid thermal CVD. Scanning electron microscope (SEM) micrographs of the resulting surfaces show profound roughness in the sample with isolated nuclei at ~1/2 area coverage on the surface. Further, the growth of nuclei with time as a function of temperature, ranging from 510°C to 570°C, at a pressure of 1.6 mTorr is depicted in Figure 4, which shows clearly that the surface area coverage by Si dots can be appropriately controlled.

Another application is shown in Figures 5(a) through 5(d), namely the formation of Si quantum dots for light emitting structures, for which the process sequence consists of the following steps:

1. An oxide layer 41 about 200 Å thick is deposited onto the surface of a substrate 40 to form the structure shown in Figure 5(a).
   This oxide can be thermally grown if the substrate material is silicon. For other substrate materials, the oxide layer can be deposited by chemical vapor deposition on top of the substrate. If a material other than oxide is necessary to mask the substrate during the subsequent etching steps described below, a layer 43 of such a material can be deposited underneath the oxide layer 41.
2. Submicrometer dots 42 formed by silicon nuclei are deposited, by chemical vapor deposition using silane gas, on the surface of the oxide layer 41 to form the structure shown in Figure 5-

(b).

A given set of deposition parameters (temperature and pressure) will be chosen in order to obtain a desired nuclei density and nuclei size, respectively. For example, Figure 6 is a plot of surface area coverage by grown nuclei as a function of deposition time at a temperature of 550 °C for deposition pressures of 1.6 and 3.2 mTorr. It will be seen from this data and that of Figure 4 that the area coverage of silicon on the surface, and therefore the Si dot size, can be controlled by suitable adjustments in temperature and pressure.

It may be advantageous in this regard to deposit silicon nitride instead of silicon oxide. The nuclei density and growth rate of the nitride nuclei will be different from an oxide surface and should be determined. In addition, the substrate surface can be treated in-situ before the deposition of the nuclei, for example, by carbon exposure or by locally etching certain areas of the oxide surface, in order to control the location of these nuclei centers and/or to further modify the nuclei density.

3. The pattern of silicon dots 42 can be transferred onto the underlying oxide layer 41 by selectively reactive ion etching (RIE) the unexposed oxide, using the silicon nuclei as a mask. The same pattern can then be transferred into the substrate 40 with another reactive ion etching step by using the oxide pattern as a mask and changing the etching gas composition, resulting in the configuration shown in Figure 5(c).

As indicated above, if a material, other than oxide, is necessary to mask the substrate material 40 during the etching steps, a layer 43 of such a material can be deposited, and such an interlayer etch stop material may be used below the SiO_2 layer to maintain the dot pattern, after selective removal of the SiO_2 between the Si dots, and then to transfer the dot pattern into the Si substrate.

4. Finally, the remaining oxide and silicon nuclei are etched away leaving the nanometer-size Si dot (44) structure shown in Figure 5(d).

Summary considerations

The low pressure conditions needed for this invention are readily achievable in ultrahigh-vacuum (UHV) CVD reactors suited for low temperature epitaxy (typically batch reactors), as well as in UHV/CVD single-wafer rapid thermal CVD reactors. Reactors of both types are available commercially and may be selected as appropriate by those of skill in the art.

Results were obtained as the result of work carried out in the latter-type reactor, and demonstrated the growth of rough Si surfaces over a broad temperature range (~100 °C), with controllable nuclei density (grain size) and nuclei shape. Apparent roughness enhancement of at least 2-3X has been demonstrated for growth on both thin thermal (device) oxide surfaces and on surfaces with only a very thin chemical oxide (prepared by standard wet cleaning procedures). Finally, it has also been demonstrated that rough Si surfaces can be grown using batch hot-wall UHV/CVD reactors. Since up to 50-100 wafers can be simultaneously processed in this way, this process opens the door to high throughput manufacturing.

As Si CVD growth typically exhibits some selectivity, it is clear that a variety of Si-containing reactants can be used for deposition, such as disilane, dichlorosilane, etc. Furthermore, it is contemplated that other surface insulators could be employed directly, such as aluminum oxide or a variety of glass materials. If desired, the bulk substrate and insulating nucleation surface materials may be different, e.g., the process could be begun with a bulk glass substrate; on which a thin SiO_2 film is deposited, and the rough Si may then be nucleated on the SiO_2.

It will be seen that the present invention offers significant advantages as compared with the prior art in the fabrication of rough Si surfaces. As noted above, the mechanism differs substantially from that which exploits growth at the amorphous/crystalline transition temperature, where serious manufacturability concerns are raised by the necessity of working with ≤10 °C process window.

Another known path to producing rough Si is to employ thermal oxidation of polySi, which is considerably faster at doped grain boundaries than into the grains. However, this approach appears to have achieved only 1.34X area enhancement so far (See, P. C. FAZAN AND A. DITALI, "Electrical characterization of textured interpoly capacitors for advanced stacked DRAMs", IEDM 90-663, 27.5.1, 1990. (Micron Technol. Corp.)). Also, relatively high temperatures are required for thermal oxidation, and lower thermal budgets which maintain amorphous Si structure are not usable, as the thermal oxidation will inevitably cause Si grain growth, leading to large-grain structures.

Another alternative is to use plasma generation of particles to form a roughness template and then to transfer that roughness pattern into the surface by anisotropic selective etching, e.g., RIE (see IBM TDB of G. S. SELWYN ET AL cited above). However, this approach is limited to rough Si formation only on top surfaces due to plasma directionality. This prevents deposition of rough Si on sidewalls, making it unusable for current DRAM designs which always exploit extensive sidewall area in

either stacked or trench capacitor geometries.

Claims

1. A method for fabricating a rough Si surface texture comprising the steps of:
providing a low-pressure CVD environment for the deposition of Si from a Si-deposition-producing gas;
providing a surface, preferably an oxide layer, that is at least one of (a) relatively unreactive to the Si-deposition-producing gas at the operating temperatures to be used in the deposition process, and (b) conditioned such that the initial Si growth is nucleation-controlled; and
performing the deposition of Si onto said surface at a pressure in the range from about 0.1 mTorr to about 100 mTorr, preferably in the range ~1 to 5 mTorr, and a temperature in the range from about 450 °C to about 700 °C, preferably in the range of 500 - 600 °C, to selectively nucleate on distinct sites on said surface.

2. Method as in claim 1 wherein said surface is conditioned by the deposition of impurities from at least one of gas phase exposure, liquid exposure, and physical vapor deposition, or
wherein said surface is conditioned by the creation of defects therein by at least one of ion implantation, x-ray radiation, ion etching/bombardment, and UV light to break surface bonds, or
wherein said surface is conditioned by the chemical modification of the surface by the growth of incomplete or defective layers thereon, or
wherein said surface is conditioned by the growth of a full surface layer comprising at least one of a native oxide, thermal oxide, CVD nitride, and plasma-enhanced CVD (PECVD) dielectric.

3. Method as in claim 1 or 2 further comprising the step of selectively growing Si on the distinct nucleation sites for enhancing and transferring the morphology pattern of the nucleation sites into a thicker, rough Si surface texture.

4. A method for fabricating trench, stacked, or planar capacitor structures with high capacitance density, comprising the steps of:
treating the surface of a substrate structure so as to render it relatively inert with respect to reaction with Si-containing species;
depositing Si nuclei on said surface and controlling the density of said Si nuclei formed on said surface by regulating the temperature and pressure conditions of said deposition;
growing on said nuclei further Si in order to produce a nearly continuous film of Si with rough surface texture on said substrate structure;
producing a thin conformal dielectric over said rough Si surface; and
depositing a Si top electrode over said dielectric to complete the capacitor structure,
wherein the step of treating the surface of a substrate structure comprises preferably the forming an oxide layer thereon.

5. A method for fabricating a surface of controlled roughness suitable, for example, as an under-layer for low-stiction thin magnetic disk surfaces, comprising the steps of:
providing a substrate of a material having a surface that is substantially inert with respect to reaction with Si-containing species;
depositing a layer of silicon on said substrate surface, said silicon layer preferably comprises a series of random Si islands, by ultra-high-vacuum chemical-vapor-deposition (UHV-CVD) so as to selectively nucleate on distinct sites; and
controlling the roughness of said silicon layer by selecting appropriate deposition parameters for the density and size of said nucleation, whereby an under-layer is formed upon which a magnetic material may be conformally deposited to produce a low-stiction magnetic surface.

6. Method as in claim 5 further comprising the step of conformally depositing a layer of magnetic material on said silicon layer to produce a low-stiction thin magnetic disk surface on said substrate.

7. A magnetic disk comprising:
a substrate having a surface that is substantially inert with respect to reaction with Si-containing species;
a layer of silicon formed on said substrate surface so as to selectively nucleate on distinct sites to a given roughness; and
a layer of magnetic material conformally deposited over the Si layer, forming a low-stiction magnetic surface on said substrate.

8. A method for fabricating a rough Si film comprising the steps of:
treating the surface of a substrate to render it relatively inert with respect to reaction with Si-containing species;
initially depositing silicon nuclei on said substrate surface to selectively nucleate on dis-

tinct sites; and
selectively growing silicon by deposition on the distinct nucleation sites to enhance and transfer the morphology pattern of the nucleation sites into a thicker, rough Si film,
wherein the roughness of said silicon film is preferably controlled by selecting appropriate deposition parameters for the density and size of said nucleation.

9. Method as in claim 8 wherein said appropriate deposition parameters comprise a pressure in the range from about 0.1 mTorr to about 100 mTorr, and/or
a temperature in the range from about 450 °C to about 700 °C.

10. Method as in claim 8 or 9 wherein said treating step comprises rendering said substrate surface substantially inert with respect to Si and silane at high temperature, preferably by forming an oxide layer on said substrate surface.

11. Method as in any one of the claims 1 to 6 and 8 to 10 wherein said deposition is by ultra-high-vacuum chemical-vapor-deposition (UHV-CVD).

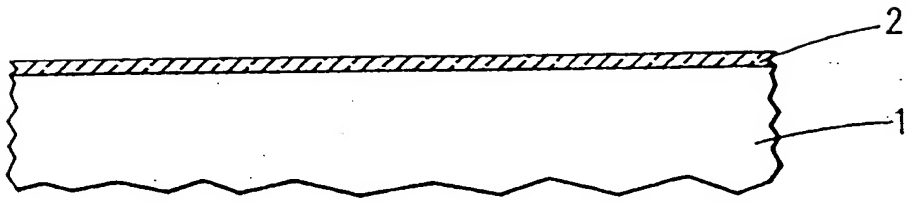

FIG. 1A

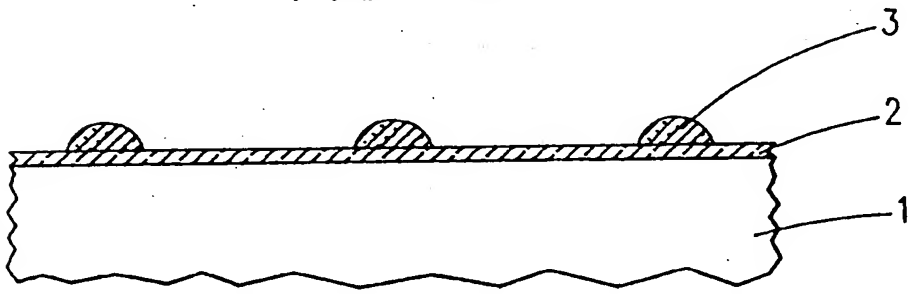

FIG. 1B

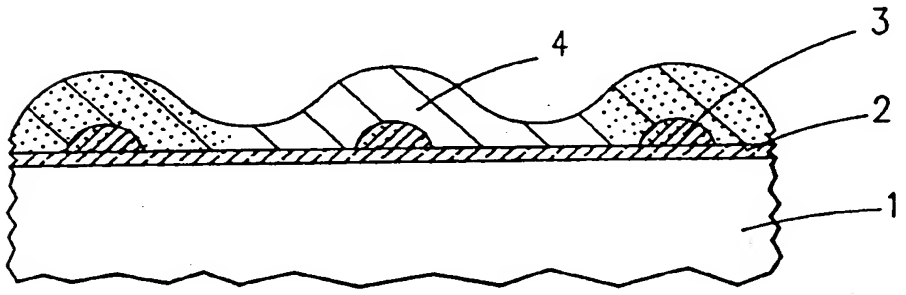

FIG. 1C

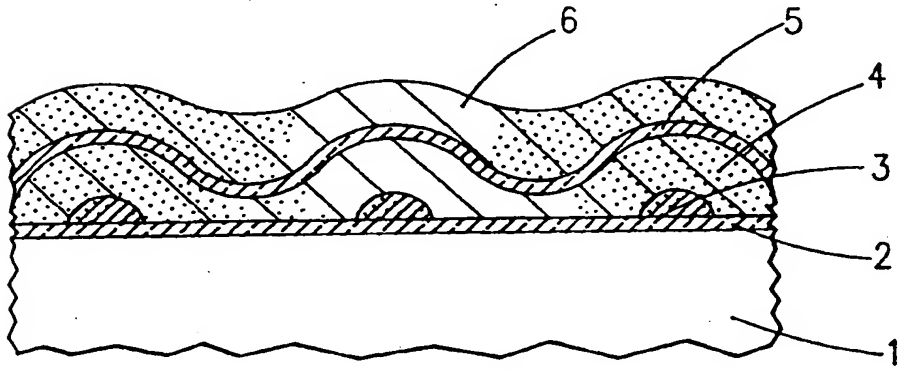

FIG. 1D

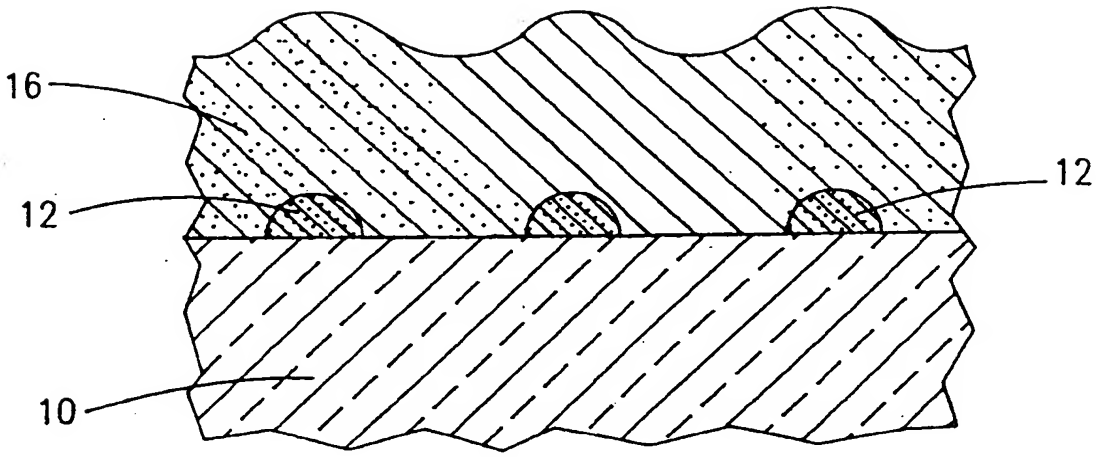

FIG.2

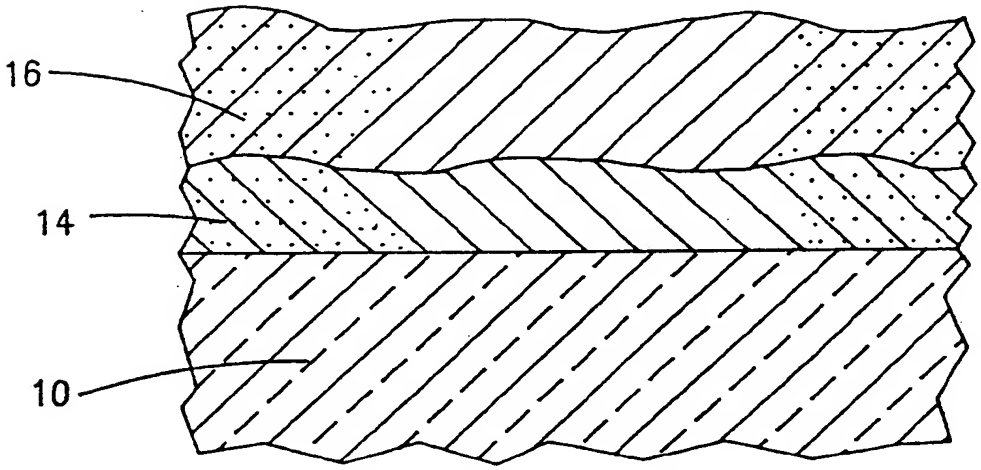

FIG.3

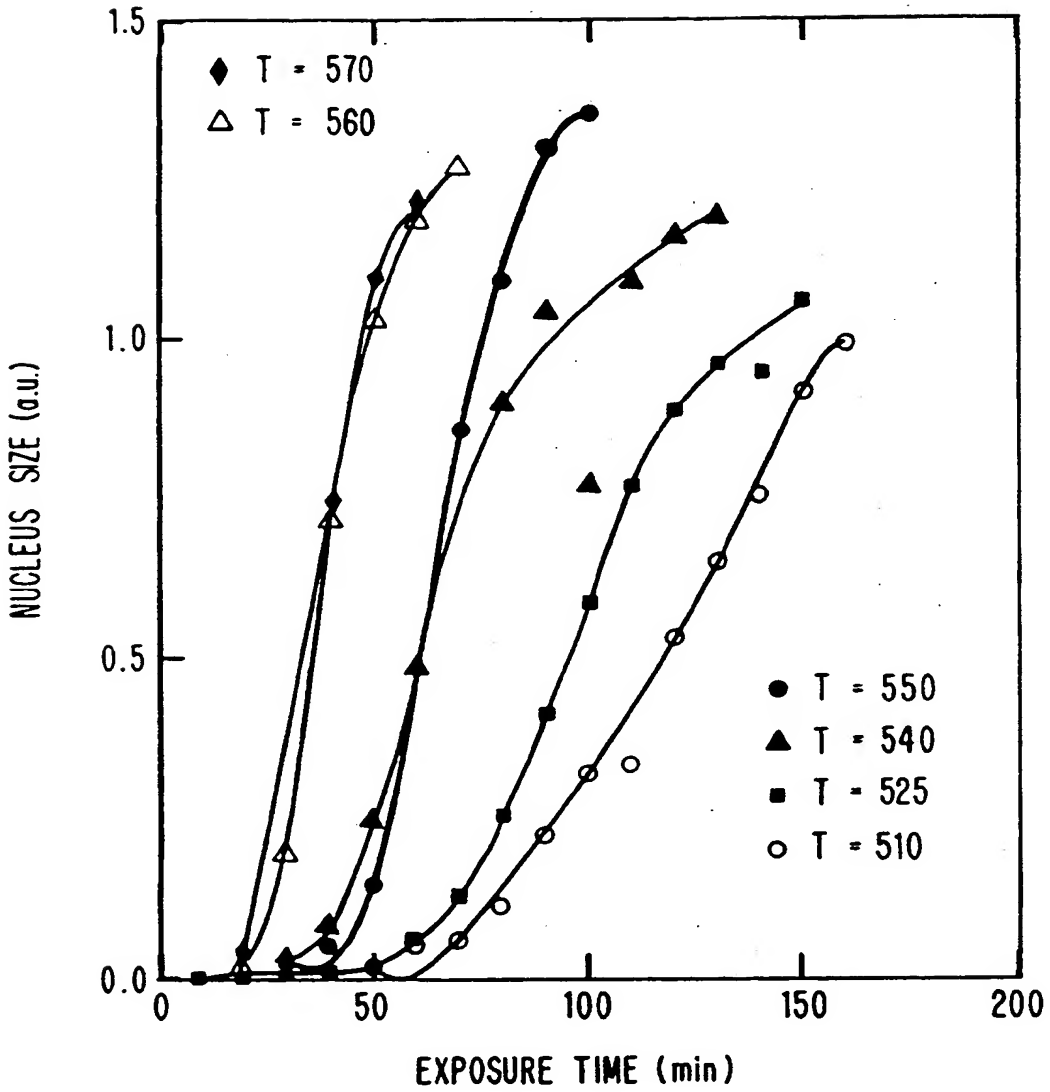

FIG. 4

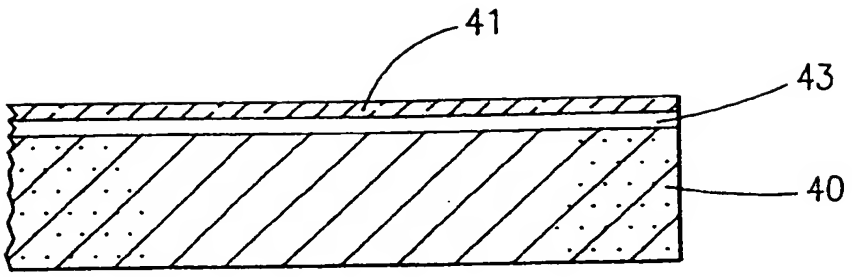

FIG.5A

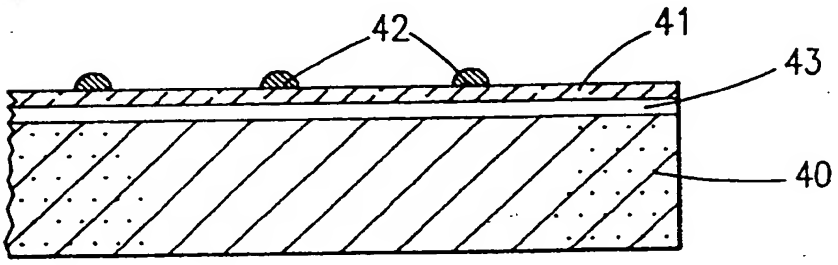

FIG.5B

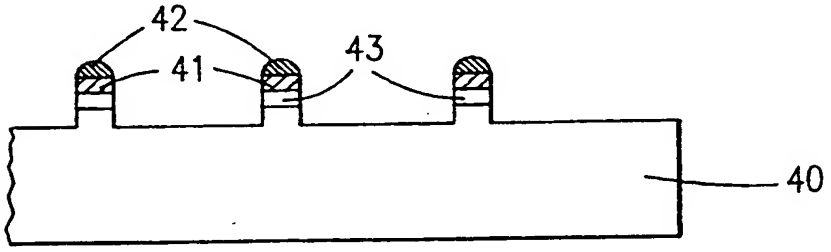

FIG.5C

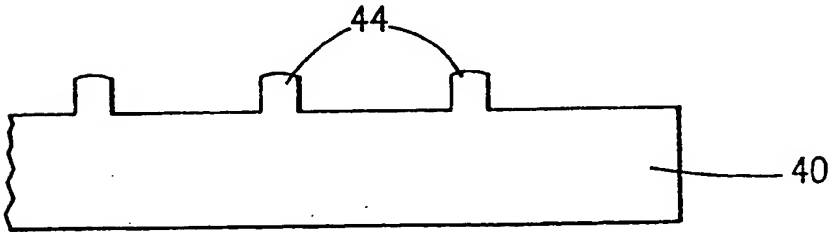

FIG.5D

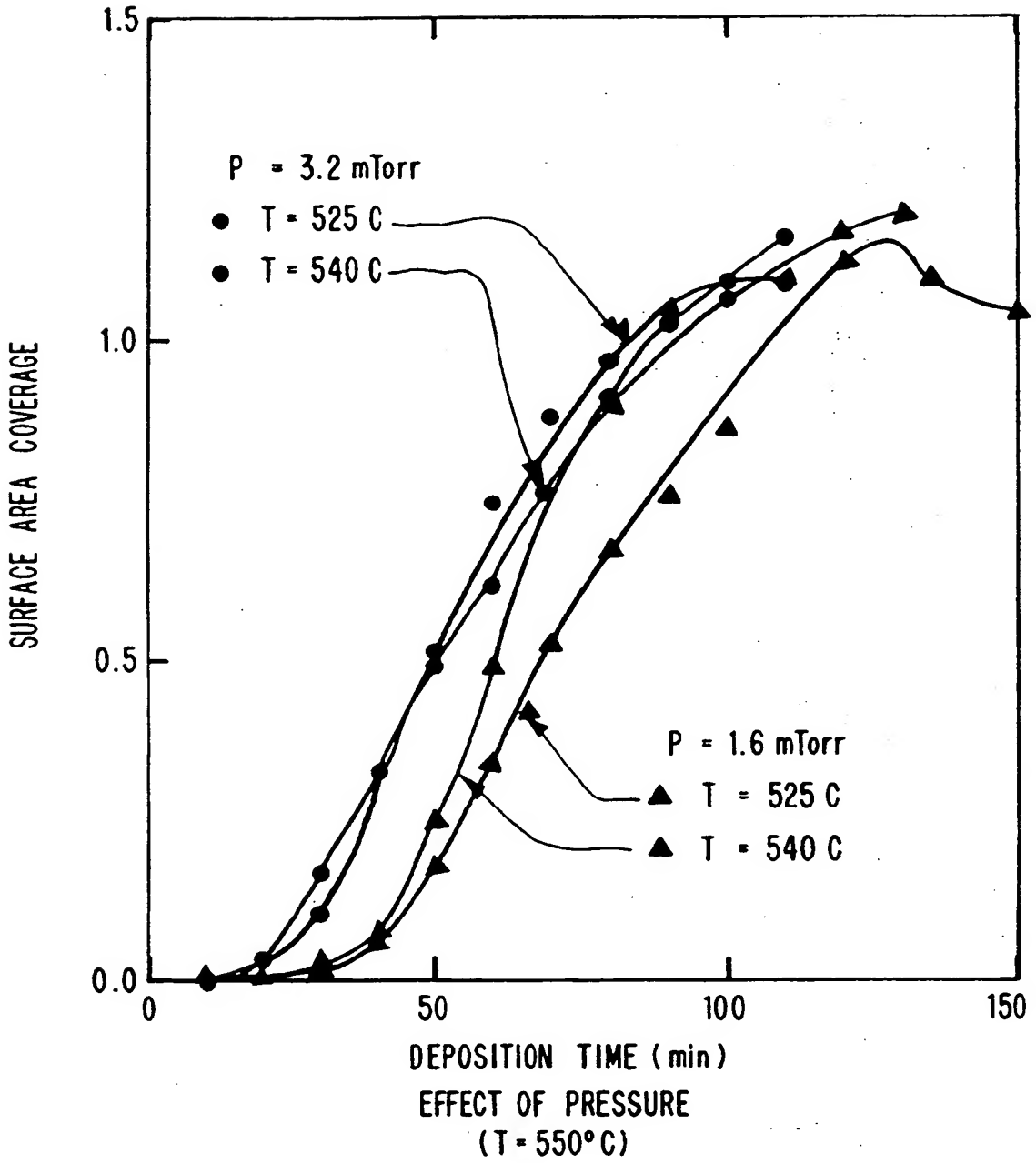

FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 4070
Page 1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	US-A-5 112 773 (MICRON TECHNOLOGY) * column 2, line 53 - line 57; figures *	1-11	G11B5/64 H01L21/3205
Y	US-A-5 102 832 (MICRON TECHNOLOGY) * abstract; figures 1-3 *	1-11	
Y	PATENT ABSTRACTS OF JAPAN vol. 16, no. 14 (E-1154)14 January 1992 & JP-A-32 34 051 (MATSUSHITA ELECTRON) 18 October 1991 * abstract * * Figure 3a-3c of original document *	1-11	
Y	JAPANESE JOURNAL OF APPLIED PHYSICS vol. 29, no. 12, December 1990, TOKYO JP pages 2345 - 2348 Y. HAYASHIDE ET AL. 'Fabrication of Storage Capacitance-Enhanced Capacitors with a Rough Electrode' * page 2345, column 1, paragraph 3 - column 2, paragraph 2; figures 1,3 *	1-11	
A	PATENT ABSTRACTS OF JAPAN vol. 15, no. 405 (E-1122)16 October 1991 & JP-A-31 65 552 (SONY CORP) 17 July 1991 * abstract * * Figure 3D - 3G of original document *	1-11	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H01L G11B
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 73 (E-1169)21 February 1992 & JP-A-32 63 370 (MITSUBISHI ELECTRIC CORP) 22 November 1991 * abstract *	1-11	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 JULY 1993	SINEMUS M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	PATENT ABSTRACTS OF JAPAN vol. 16, no. 246 (E-1212)5 June 1992 & JP-A-40 51 564 (FUJITSU LTD) 20 February 1992 * abstract *	1-11	
A	PATENT ABSTRACTS OF JAPAN vol. 12, no. 412 (E-676)31 October 1988 & JP-A-63 151 069 (MATSUSHITA ELECTRIC) 23 June 1988 * abstract *	1-11	
A	US-A-5 091 225 (NEC CORP) * column 1, paragraph 2; figure * * abstract *	5-7	
A	DE-A-3 543 254 (SIEMENS) * abstract; figures *	5-7	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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